Amendments to the Specification:

Please replace the Abstract of the application with the following amended Abstract:

A bipolar transistor is disclosed that is produced using a sacrificial mesa disposed over a layer of Si and SiGe in order to prevent a polysilicon covering layer from forming over a predetermined region of the Si and SiGe layer forming the transistor base. After an etching process, the sacrificial mesa is removed and the Si and SiGe layer is exposed, where an oppositely doped material is applied over top of the Si and SiGe layer to form an emitter. This makes it possible to realize a thin layer of Si and silicon germanium to serve as the transistor base. The transistor device formed using the sacrificial mesa results in the base layer Si and SiGe [from] not being affected by a process of etching, as it otherwise would be using a conventional double-poly process, which results in a more repeatable bipolar transistor device yield.

Please replace paragraph 0062 of the application currently on file with the following paragraph 0062:

[0062] An essential step in a manufacturable epitaxial process is the reproducible deposition of epitaxial silicon and/or SiGe on a mixed topography i.e. single crystal silicon, poly Si, and oxide (or nitride) of variable roughness. This invention discloses a method for deposition of a seed layer atop the collector region to form a planar surface and a thin uniform thickness, continuous interconnecting silicon or silicon germanium layer without pinholes and defect free. The term thickness is understood by those of skill in the art as a [thickness] height of a layer in a direction transverse the layers within the semiconductor substrate [perpendicular to a plane of a surface of a wafer on which the layer is formed]. Turning now to Figs. 3b and 3c a preferred embodiment of the invention is shown wherein a nucleation seed layer of Si or SiGe is applied over a mixed topology of layers shown, comprising poly-silicon 101, a section 103 of the region 102 of SiO_2, and the silicon substrate 110. This is accomplished at ultra low pressure and ultra-low flow rates to provide adequate time for nucleation of the deposited layer on all surfaces; oxide, nitride, polysilicon, epitaxial silicon and SiGe. Smooth deposited layers of uniform

thickness with continuous coverage of all surfaces is possible using this method. In order to have the continuous film or seed layer deposit and nucleate over the entire region of the dissimilar materials such as dielectric material and semiconductor material, it is important to meet several conditions. Deposition must be performed at a low temperature below 600 °C, a low pressure of less than 10^{-2} mbar, and at low flow rate of less than 5 cm^3/min. Another advantage to this method, is that in a mixed topography wherein relatively different sized Si and oxide regions exist, by depositing a seed layer in accordance with the teachings of this invention over top of these regions, at low temperature, pressure and flow rate, loading effects are substantially minimized when the SiGe layer is deposited upon the seed layer. Seed layers have been discussed in the prior art, however these layers have not achieved a desired effect of nucleating a continuous film over a large region of dissimilar materials including dielectrics and semiconductors. Furthermore, prior art seed layers are applied at higher temperatures, flow rates and pressure than are taught in this invention in order to increase the throughput. Surprisingly, it was discovered by the inventors of this invention, that lowering the temperature, pressure and flow rate allowed nucleation that would not otherwise occur. Without the seed layer no deposition on oxide or nitride surfaces is possible thereby resulting in a discontinuous film of silicon or SiGe over mixed surface topography which would substantially increase R_h. Planarization of the prior surfaces reduces roughness and removes prior process deficiencies. Residual patches of silicon dioxide or carbon-containing material on the exposed silicon window surface can result in defects during post epitaxy processing by injecting dislocations and other defects such as stacking faults. The seed layer drastically reduces this tendency by introducing a planar surface coverage thereby removing the stress concentration at any heterogeneity in the interface and at discontinuities in the surface, for example silicon/silicon dioxide/poly silicon.